forming leads used in the data lines and the peripheral circuit by using a third conductive layer;

forming the pixel electrode electrically connected to the conductive interlayer; and

forming a storage capacitor for each pixel electrode, and the conductive interlayer being disposed between the switching element and the data line, and functioning as a part of an electrode constituting the storage capacitor.

REMARKS

Claims 1, 2, 4-7 and 9-33 are pending. By this Amendment, claims 1, 2, 7, 23, 24, 32 and 33 are amended. Reconsideration based on the above amendments and the following remarks is respectfully requested.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Applicant gratefully acknowledges the courtesies extended to Applicant's attorney during the January 14 personal interview with Examiner Parker. The points discussed during the interview are re-emphasized in this Amendment.

I. Rejection Under 35 U.S.C. §112, second paragraph

Claim 24 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claim 24 is amended to obviate this rejection, and accordingly withdrawal of the rejection under 35 U.S.C. §112, second paragraph is respectfully requested.

II. Rejection under 35 U.S.C. §103

Claims 1, 2 and 4-5 stand rejected under 35 U.S.C. §103(a) over Moon (U.S. Patent No. 6,133,967) in view of Kouchi (U.S. Patent No. 5,886,365), Aoki (U.S. Patent No. 6,177,916) and Sato (U.S. Patent No. 6,081,305); claims 1, 2 and 4-5 stand rejected under 35 U.S.C. §103(a) over Nakagaki (U.S. Patent No. 6,104,370) in view of Kouchi, Aoki

and Sato; claims 1, 2 and 4-5 stand rejected under 35 U.S.C. §103(a) over Fujihara (U.S. Patent No. 5,771,083) in view of Kouchi, Aoki and Sato; claims 6-7 and 9-33 stand rejected under 35 U.S.C. §103(a) over Fujihara in view of Kouchi, Aoki and Sato and further in view of Mizuno (U.S. Patent No. 6,266,110), Someya (U.S. Patent No. 5,838,399) and Aoki (U.S. Patent No. 5,425,857, hereinafter Aoki '857); claims 6-7 and 9-33 stand rejected under 35 U.S.C. §103(a) over Nakagaki, Kouchi, Aoki and Sato and further in view of Mizuno, Someya and Aoki '857; claims 6-7 and 9-33 stand rejected under 35 U.S.C. §103(a) over Moon in view of Kouchi, Aoki and Sato and further in view of Mizuno, Someya and Aoki; and claims 6-22 stand rejected under 35 U.S.C. §103(a) over Kouchi, Aoki or Sato in view of Mizuno, Someya and Aoki '857. Applicant respectfully traverses the rejections.

In particular, none of the applied references disclose or suggest an electro-optical device including a conductive interlayer that electrically connects a corresponding switching element and a corresponding pixel electrode the conductive interlayer being disposed between the switching element and the data line, and functioning as a part of an electrode constituting the storage capacitor, as recited in independent claim 1, and similarly recited in independent claims 23, 32 and 33.

Further, none of the applied references disclose or suggest an electro-optical device including first, second, and third conductive layers, formed in that order, the third conductive layer having a resistance which is lower than the resistance of the first conductive layer, one interlayered insulation layer being disposed between the first and second layers and another interlayered insulation layer being disposed between the second and third conductive layers, a peripheral circuit which is provided with leads comprising a first, second and third conductive layers and drives each switching element peripheral circuit having parallel leads in which a lead comprising a first conductive layer and a lead comprising a second

conductive layer electrically connected in parallel with respect to both ends of the parallel leads, as recited in independent 6.

Moon discloses a liquid crystal display including a thin film transistor (TFT) and a storage capacitor where a gate insulating layer 5 is selectively etched using a gate electrode 3 as a mask. A dielectric layer 6 is formed of the substrate. A conductive layer is deposited thereon and patterned to form a storage electrode 4. High-concentration impurities are doped into a predetermined portion of the active layer 1 to form source and drain regions, which are indicated by a new part of impurity-dope semiconductor layer 2. The dielectric layer 6 together with the impurity-dope semiconductor layer 2 and the storage electrode 4 constitutes a storage capacitor. See, for example, Figs. 2A - 2E and col. 4, lines 14-30.

However, Moon fails to disclose or suggest a conductive interlayer that electrically connects the corresponding switching element and corresponding pixel electrode where the conductive interlayer being disposed between the switching elements and the data line, and functioning as part of an electrode constituting the storage capacitor.

Nakagaki discloses a silicon substrate 1 including a MOSFET 2 having a drain 5, a gate 6 and a source 7, and a capacitor 3 for storing electric charge corresponding to one pixel. An aluminum pixel electrode layer 8 is formed on the insulator layer 4. A lower portion of the pixel electrode 8 is connected to the source 7 of the MOSFET 2. A conductor 9 extends sideways from the connecting portion. An SIO_2 dielectric film 10 is intervened between the substrate 1 and the conductor 9. This lamination constitutes the capacitor 3. See, for example, Fig. 7 and col. 4, lines 49-60.

However, Nakagaki fails to disclose or suggest a conductive interlayer that electrically connects the corresponding switching element and correspond pixel electrode where the conductive interlayer being disposed between the switching element and the data line, and functioning as a part of an electrode constituting the storage capacitor.

Fujihara discloses a structure of an active matrix substrate in a liquid crystal display device where the storage capacitor line 4 and the oxide insulating films 9 are formed on the light transmitting substrate 1. In addition, the gate insulating film 10 is formed to cover all of the members. The source signal line 3 is arranged on the gate insulating film 10. The inter-layer insulating film 14 is formed on the source signal line 3. Furthermore, the pixel electrode 5 is produced on the inter-layer insulating film 14. See, for example, Fig. 3 and col. 6, lines 24-34.

However, Fujihara fails to disclose or suggest a conductive interlayer that electrically connects the corresponding switching element and corresponding pixel electrode where the conductive interlayer being disposed between the switching element and the data line, and functioning as part of an electrode constituting the storage capacitor.

Furthermore, neither Kouchi, Aoki, Sato, Mizuno, Someya nor Aoki '857 cure the above-noted deficiencies of Moon, Nakagaki and Fujihara.

Kouchi discloses a small size and large capacitance capacitors are provided for the peripheral driving circuit of a liquid crystal display device. The capacitor exhibiting crystalline properties is provided on a monocrystalline silicon in a peripheral driving circuit using an insulator film deposition process used to manufacture TFTs of a display pixel portion in a peripheral driving circuit. The capacitor, using monocrystalline silicon as electrodes and an insulator on the monocrystalline silicon as a dielectric, has a small size and a large capacitance as compared with a capacitor manufactured on amorphous silicon or monocrystalline silicon and is thus capable of high quality display. See, for example, Abstract of Kouchi.

Aoki discloses buffer circuits and analogue switches are disposed closer to a display region than video busses. A timing signal generator circuit provides the buffer circuits with a timing signal. The analogue switches supply video signals from the video busses to signal

lines in a display region in response to the timing signal. Parasitic capacitance coupled to the video busses is reduced so that bandwidth characteristics of the busses can be improved and a good display can also be obtained. See, for example, Abstract of Aoki.

Sato discloses a liquid crystal light valve used for a projection type display where in a pixel circuit MOS transistors 1A and holding capacitors 1B are arranged in M lines in a horizontal direction and in N rows in a vertical direction respectively (see Fig. 9). The scanning signals and brightness signals are inputted into the gate electrodes and the drain electrodes of the MOS transistors through first signal lines and second signal lines, respectively, and each of the source electrodes is connected to one end of a holding capacitor 1B and one end of a liquid crystal element 1C. See, for example, col. 4, lines 20-35.

Mizuno discloses an uppermost metal wiring layer is formed of titan Ti and titan nitride TiN formed thereon, on which tungsten W for filling a via hole can be deposited. The via hole is filled with W. The surface of a metal wiring layer below the uppermost metal wiring layer is covered with a low reflectivity film made of titan nitride. Thus, light incident on the surface of the semiconductor chip is prevented from reaching a substrate transistor within a semiconductor device and malfunctioning of the semiconductor device is prevented. See, for example, Abstract of Mizuno.

Someya discloses a TFT active matrix liquid crystal display devices in which a pixel is divided into three parts, a capacitor is added to each pixel, light shielding is applied to each TFT, and the matrix is driven by a DC canceling technique. See, for example, Abstract of Someya.

Aoki '857 discloses a matrix type display having a TFT substrate where a gate signal line interconnects respective gate electrodes of the TFTs arranged in a row or column of the matrix array, a source electrode line interconnecting respective source or drain electrodes of TFT arranged in a column or row of the matrix array, a pixel electrode form of a transparent

conductor film and connected to the source or drain electrode of each of the TFTs, a capacitor electrode capacitively coupled to the pixel electrode through a dielectric film, a conductor wire interconnecting the respective capacitive electrode of the pixels interconnected by the gate signal line, wherein the conductor wire is formed integrally with the capacitor electrode. See, for example, Abstract of Aoki '857.

Furthermore, none of the applied references for reasons as stated above, disclose or suggest a first, second and third conductive layers and drives each switching element peripheral circuit having parallel leads in which a lead comprising the first conductive layer and a lead comprising the second layer electrically connected in parallel with respect to both ends of the parallel leads, as recited in independent claim 6.

Accordingly, Applicant submits that independent claims 1, 6, 23, 32 and 33 define patentable subject matter. Claims 2 and 4-5 depend from the independent claim 1, claims 7 and 9-22 depend from independent claim 6, claims 24-31 depend from independent claim 23, therefore also define patentable subject matter. Accordingly, Applicant requests that the rejections under 35 U.S.C. §103(a) be withdrawn.

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-2, 4-7 and 9-32 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number set forth below.

Respectfully submitted,

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JAO:YSC/sdb

Attachment:
Appendix

Date: January 21, 2003

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Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claims:

1. (Twice Amended) An electro-optical device, comprising:

a plurality of scanning lines and a plurality of data lines;

a combination of a switching element and a pixel electrode provided corresponding to each crossing between the scanning lines and the data lines, each pixel electrode being electrically connected to ~~provided with~~ a storage capacitor ~~of which a first end is connected to the pixel electrode and a second end is commonly connected~~;

a conductive interlayer that electrically connects the corresponding switching element and the corresponding pixel electrode, the conductive interlayer being disposed between ~~an interlayered insulation layer, which is disposed on said switching element,~~ the switching element and the data line, ~~and said pixel electrode in a lamination structure of said electro-optical device~~ and functioning as a part of an electrode constituting the storage capacitor; and

a peripheral circuit containing leads that comprises the same layer as the conductive layer constituting the conductive interlayer, and drives the switching element.

2. (Amended) The electro-optical device according to claim 1, the conductive interlayer being electrically connected to an electrode of the switching element via a first contact hole provided corresponding to the electrode, whereas the pixel electrode is electrically connected to the switching element via a second contact hole.

7. (Amended) The electro-optical device according to claim 6, the conductive interlayer being electrically connected to an electrode of the switching element via a first contact hole provided corresponding to the electrode, whereas the pixel electrode is electrically connected to the switching element via a second contact hole.

23. (Twice Amended) An electro-optical device, comprising:

a plurality of scanning lines and a plurality of data lines;

a combination of a switching element and a pixel electrode provided corresponding to each crossing between the scanning lines and the data lines, each pixel electrode being electrically connected to ~~provided with~~ a storage capacitor ~~of which a first end is connected to the pixel electrode and a second end is commonly connected~~;

a conductive interlayer that electrically connects the switching element and the corresponding pixel electrode, the conductive interlayer being disposed between the switching element and the data line~~an interlayered insulation layer, which is disposed on said switching element~~, and ~~said pixel electrode in a lamination structure of said electro-optical device and~~ functioning as a part of an electrode constituting the storage capacitor;

a peripheral circuit for driving the switching element; and

leads connected to the peripheral circuit that comprise the same layer as a conductive layer which constitutes the conductive interlayer.

24. (Amended) The electro-optical device according to claim 23, the leads crossing ~~beneath~~ between at least one image signal line which comprises the same layer as a conductive layer which constitutes the data lines.

32. (Amended) A method for making an electro-optical device comprising a plurality of scanning lines, a plurality of data lines, and a combination of a switching element and a pixel electrode provided at a position corresponding to each crossing between the scanning lines and the data lines, the method comprising:

forming the switching element at the position corresponding to each crossing between the scanning lines and the data lines;

forming a conductive interlayer electrically connected to the switching element and leads used in a peripheral circuit for driving the switching element, by using the same conductive layer;

forming the pixel electrode electrically connected to the conductive interlayer; and

forming a storage capacitor for each pixel electrode ~~of which a first end is connected to the pixel electrode and a second end is commonly connected~~, and the conductive interlayer being disposed between ~~an interlayered insulation layer, which is disposed on said switching element~~the switching element and the data line, and ~~said pixel electrode in a lamination structure of said electro-optical device and~~ functioning as a part of an electrode constituting the storage capacitor.

33. (Amended) A method for making an electro-optical device comprising a plurality of scanning lines, a plurality of data lines, and a combination of a switching element and a pixel electrode provided at a position corresponding to each crossing between the scanning lines and the data lines, the method comprising:

after forming the scanning lines and leads used in a peripheral circuit for driving the corresponding switching element by using the first conductive layer, and forming the switching element at the positions corresponding to each crossing between the scanning lines and the data lines;

forming a conductive interlayer electrically connected to the switching element and leads used in a peripheral circuit for driving the corresponding switching element, by using a second conductive layer;

forming leads used in the data lines and the peripheral circuit by using a third conductive layer;

forming the pixel electrode electrically connected to the conductive interlayer; and

forming a storage capacitor for each pixel electrode ~~of which a first end is connected to the pixel electrode and a second end is commonly connected~~, and the conductive interlayer being disposed between ~~an interlayered insulation layer, which is disposed on said switching element~~the switching element and the data line, and ~~said pixel electrode in a lamination structure of said electro-optical device and~~ functioning as a part of an electrode constituting the storage capacitor.